PROCESS OF FABRICATING HIGH RESISTANCE CMOS RESISTOR

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a semiconductor manufacturing process, and more specifically to a process of fabricating a high resistance CMOS resistor.

Description of Related Art

[0002] Many common circuits manufactured using CMOS process require resistor elements. In the area of analog circuits, resistor elements having high-resistance values (100kΩ-500kΩ) are sometimes desired. The demand for such resistors is especially common in the field of power-relative analog circuits.

[0003] In one common application, many power-relative analog circuits include voltage dividers constructed from a pair of CMOS resistors. Such voltage dividers provide reference voltages that are stepped down from a supply voltage. The higher the resistance of the resistors is, the less standby power will be consumed.

[0004] Currently, most widely used CMOS resistors are either junction resistors or film resistors. Common junction resistor types include NW resistors, PW resistors, NDIFF(N+S/D) resistors, and PDIFF(N+S/D) resistors. Common film resistor types include Poly resistors, M1 resistors, and M2 resistors.

[0005] Though these resistors have satisfactory resistor characteristics, their resistance is generally limited to 1kΩ-5kΩ per square. When a high-resistance element is required, it can be created either by using extra die space, or by performing additional masking steps during the manufacturing process. However, neither of these

alternatives is desirable because they both increase the cost of manufacturing the circuit.

[0006] Creating a high-resistance resistor (100kΩ-500kΩ) with traditional CMOS resistors is often commercially impractical due to die-size and cost restrictions. Therefore, there exists a need for a CMOS resistor having a significantly higher resistance per square than existing CMOS resistors. Furthermore, the process for manufacturing such a CMOS resistor should not require any additional masking steps.

SUMMARY OF THE INVENTION

[0007] The present invention provides a process of fabricating a high resistance CMOS resistor with a relatively small die-size. Such a CMOS component can reduce the cost and the die-size of existing circuits to fabricate many novel CMOS circuit designs.

[0008] While current CMOS resistors generally do not exceed 1kΩ-5kΩ per square, the present invention presents a process of fabricating the high resistance CMOS resistor having a resistance of 10k-20kΩ per square. Furthermore, unlike many existing processes of fabricating CMOS resistors, the process according to the present invention does not require any additional masking steps.

[0009] According to an embodiment of the present invention, the process of fabricating a high resistance CMOS resistor comprises the following steps: An n-well and a p-well are formed in a p-type silicon substrate. Next, a nitride layer is then deposited over the p-type silicon substrate. Next, photolithography and etching steps are used to pattern the nitride layer to form a patterned mask layer for defining a non-active area and active area over the p-type silicon substrate. In general, some p-type

ions are implanted into the non-active area of the p-well. Some channel-stops are also implanted for increasing the isolation capability.

[0010] To form a CMOS resistor, the CMOS process according to the present invention includes injecting the same p-type ions into the n-well to form a p-field region. After that, a field oxide is formed on the CMOS resistor. Heavily doped p-type contact regions are formed as the ohmic contacts of the CMOS resistor, after the photolithography, etching, and implanting steps. Finally, two contact openings and two metal contact plugs are formed to electrically connect two ohmic contacts of the CMOS resistor. Thus, a high resistance resistor is formed without requiring any additional masking steps. In addition, this process is fully compatible with standard CMOS processes.

[0011] The CMOS resistor according to the present invention substantially reduces the standby power consumption of voltage dividers that are widely used for generating reference voltages. A CMOS resistor having a resistance of $10k\Omega$-$20k\Omega$ per square could also substantially reduce the manufacturing and operating costs of many other existing circuits. A higher resistance per square could also make many new analog circuit designs involving high-resistance resistors possible.

[0012] However, the scope of this invention is no way limited to the field of low standby-power electronics, or to voltage dividers. There are many other types of circuits that could potentially benefit from the use of such high-resistance CMOS resistors. Still further objects and advantages will become apparent from a consideration of the ensuing description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The accompanying drawings are included to provide a further understanding

of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0014] FIG. **1** is a cross-sectional view illustrating a step of forming an n-well in a p-type silicon substrate according to an embodiment of the present invention.

[0015] FIG. **2** is a cross-sectional view illustrating a step of forming a p-well and the n-well in the p-type silicon substrate according to an embodiment of the present invention.

[0016] FIG. **3** is a cross-sectional view illustrating a step of forming an active area in the p-type silicon substrate according to an embodiment of the present invention.

[0017] FIG. **4** is a cross-sectional view illustrating a step of forming a p-field area in the n-well and forming another p-field area in the p-well according to an embodiment of the present invention.

[0018] FIG. **5** is a cross-sectional view illustrating a step of performing a field oxidation process according to an embodiment of the present invention.

[0019] FIG. **6** is a cross-sectional view illustrating a step of forming an n-type contact region according to an embodiment of the present invention.

[0020] FIG. **7** is a cross-sectional view illustrating a step of forming two p-type contact regions according to an embodiment of the present invention.

[0021] FIG. **8** is a cross-sectional view illustrating steps of forming two metal contact plugs, and a passivation layer according to an embodiment of the present invention.

DESCRIPTION OF THE EMBODIMENTS

[0022] Referring now to the drawings wherein the contents are for purposes of illustrating the preferred embodiment of the invention only and not for purposes of

limiting the same. Referring to FIG. **1**, phosphorus ions are implanted in a p-type silicon substrate **20** to form an n-well **22**. The p-type silicon substrate **20** is doped with boron ions to achieve a resistance of 8Ω-12Ω per cm. The n-well **22** can be formed via well-known photolithography, etching and implantation process as follows. A photoresist layer is formed over the p-type silicon substrate **20**. Next, the photoresist layer is exposed using a mask to expose predetermined portions of the photoresist layers. Next, the exposed photoresist is etched to remove the predetermined portions of the p-type silicon substrate **20**. Next, an ion implementation is then carried out using an energy level of 100 KeV using phosphorus ions with a dosage level ranging from $6x10^{12}$ to $9x10^{12}$ ions/cm^2.

[0023] Next, as FIG. **2** shows, boron ions are implanted into the p-type silicon substrate **20** to form a p-well **30**. The implantation is done using an energy level of 40 KeV, with a dosage level ranging from $8\ x10^{12}$ to $9x10^{12}$ ions/cm^2. Next, a thermal annealing process is carried at, for example, a temperature of about 1150℃, to diffuse the n-type and p-type ions into the respective regions within the p-type silicon substrate **20**.

[0024] As shown in FIG. **3**, a pad oxide layer **40** having a thickness of about 350 angstroms is formed over the surface of the p-type silicon substrate **20**. The pad oxide layer **40** is formed, for example but limited to, by performing a thermal oxidation at a temperature of 900℃. Next, a nitride layer having a thickness of 1250 angstroms is then deposited at a temperature of 850℃ over the pad oxide layer **40**. Next, the nitride layer is etched via photolithography and etching process to form a patterned mask layer **42** over the surface of the pad oxide layer **40**. The patterned mask **42** serves as a mask in the subsequent process.

[0025] Hereinafter, as FIG. **4** shows, performing an ion implantation process **46** using the patterned mask layer **42** as the mask forms a p-field region **50** and a p-field region **52**. Boron ions are then implanted at an energy level of 50KeV with a dosage level ranging from $4x10^{13}$ to $6x10^{13}$ ions/ cm^2.

[0026] As shown in FIG. **4**, the p-field region **50** and the p-field region **52** are formed below the pad oxide layer **40**. As it will be well known to those skilled in the art that the p-field implantation is a standard CMOS process. In general, the p-field region **50** is implanted into the p-well **30**. The p-field region **50** acts as device isolation layers (ie, channel stops). However, it should be understood that the p-field implantation could also be done in an unconventional manner. The p-field region **52** is implanted into the n-well **22** in order to form a window into the n-well **22**. The p-field region **52** forms a CMOS resistor. This step enables the CMOS resistor, according to the present invention, to be built without the use of any additional masking steps. A field oxidation process is performed at a temperature of 980℃ to form a field oxide layer **60** over the p-type silicon substrate **20** as shown in FIG. **5**. The field oxide layer **60** is grown to a thickness of about 5000-6000 angstroms. When this step is completed, the patterned mask layer **42** will be removed.

[0027] Now turning to FIG. **6**, an n-type contact region **70** is formed in the n-well **22**. For example, the n-type contact region **70** can be formed via a conventional photolithography and etching process to form a patterned mask layer exposing predetermined portion of the n-well **22**. Arsenic ions are implanted at an energy level of 80 KeV, with a dosage level in a range of $4x10^{15}$ to $6x10^{15}$ ions/cm^2. The implantation is done with heavier arsenic atoms because this forms the n-type contact region **70** with a shallow depth. This forms a window for the field oxide layer **60**.

[0028] As shown in FIG. **7**, after forming the n-type contact region **70**, p-type contact regions **80** and **82** are formed in the n-well **22**. Similarly, the p-type contact region **80** and p-type contact region **82** can also be formed by performing conventional photolithography and etching process to form a patterned mask layer, and then using the patterned mask layer as mask. Boron ions are implanted at an energy level of 25KeV with a dosage level ranging from $2x10^{15}$ to $4x10^{15}$ ions/cm^2.

[0029] FIG. **7** shows a cross-sectional view of the p-type contact region **82** implanted in the n-well **22**. Therefore, the p-type contact region **80** and the p-type contact region **82** are formed in the n-well **22**. The p-type contact regions **80** and **82** act as two ohmic contacts of the CMOS resistor. And this completes the fabrication of a high resistance CMOS resistor.

[0030] Next, contact openings and metal contact plugs are formed to electrically contact the two ohmic contacts of the CMOS resistor. As shown in FIG. **8**, a BPSG layer **90** is deposited to form two contact openings. For example, the thickness of the BPSG layer **90** is in the range of 5,000 to 8,000 angstroms. Subsequently, a metal layer **92** having a thickness of 5,000 angstroms is sputtered over the BPSG layer **90**. For example, the metal layer **92** is an AlSiCu layer. Finally, an oxide layer **94** having a thickness in the range of 5,000 to 10,000 angstroms is deposited over the resulting structure. The oxide layer **94** serves as a passivation layer to protect the CMOS resistor.

[0031] Thus, a CMOS resistor having high resistance is formed without any additional masking steps. In addition, this process is fully compatible with standard CMOS processes. This CMOS resistor will have a resistance of about 10kΩ-20kΩ per square.

[0032] It is to be understood that this process of fabricating a CMOS resistor according to the present invention is described for the purpose of illustrating rather than limiting the scope of the present invention.

[0033] Thus, it will be apparent to those skilled in the art, that the method for manufacturing a CMOS resistor according to the present invention could also be applied to manufacture an n-field resistor in an n-type silicon substrate, without departing from the spirit or the scope of thé invention.

[0034] In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims or their equivalents.